1. (Currently amended) A semiconductor imaging chip comprising:

an array of active pixel sensors arranged in rows and columns, each of said active pixels sensors having a respective active pixel sensor signal value and an active pixel sensor reset value;

an output terminal; and

a plurality of multiplexed column buffers, each of said plurality of multiplexed column buffers having a respective first plurality of input terminals coupled to a respective first plurality of said columns, each of said plurality of multiplexed column buffers ~~and a multiplexed column buffer output terminal coupled to said output terminal,~~ comprising:

first, second, third and fourth memory elements;

said first memory element adapted to store an active pixel sensor signal value for a first column of said array;

said second memory element adapted to and an active pixel sensor reset value for said first column of said array;

said third memory element adapted to store an active pixel sensor signal value for a second column of said array;

said fourth memory element adapted to and an active pixel sensor reset value for said second column of said array;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

said first input terminal of said differential gain amplifier being selectively coupled to one of said first and third memory elements;

said second input terminal of said differential gain amplifier being selectively coupled to one of said second and fourth memory elements; and

the output terminal of said differential gain amplifier being selectively coupled to said output terminal of said semiconductor imaging chip.

2. (canceled)

3. (Currently amended) A semiconductor imaging chip in accordance with claim 1, wherein each of said plurality of multiplexed column buffers ~~multiplexed column buffer~~ further comprises;

a multiplexed bus driver amplifier having respective input and output terminals;

fifth and sixth memory elements;

said fifth memory element being selectively coupled to said output terminal of said differential gain amplifier to store a corrected APS pixel signal value output for said first column of said array;

said sixth memory element being selectively coupled to said output terminal of said differential gain amplifier to store a corrected APS pixel signal value output for said second column of said array;

said input terminal of said multiplexed bus driver amplifier being sequentially coupled to said fifth memory and said sixth memory elements so as to sequentially output a corrected APS pixel signal value for said first column of said array followed by a corrected APS pixel signal value for said second column of said array.

4. (Currently amended) ~~In a~~A semiconductor imaging chip ~~having~~ comprising:

an array of active pixel sensors arranged in rows and columns;~~,~~

a plurality of multiplexed column buffers each of said plurality of column buffers being coupled to a group of columns, each of said plurality of column buffers comprising:

respective first, second, third and fourth ~~and second~~ memory elements;

respective first, second, third, fourth, fifth, sixth, seventh and eighth ~~fourth~~ switches;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

said first switch coupling said first memory element to a first column of said array of active pixel sensors;

said second switch coupling said second memory element to ~~a second~~ said first column of said array of active pixel sensors;

~~said third switch coupling said differential gain amplifier to said first memory element; and~~

~~said fourth switch coupling said differential gain amplifier to said second memory element.~~

said third switch coupling said third memory element to a second column of said array of active pixel sensors;

said fourth switch coupling said fourth memory element to said second column of said array of active pixel sensors;

said fifth switch coupling said first memory element to said first input terminal of said differential gain amplifier;

said sixth switch coupling said third memory element to said first input terminal of said differential gain amplifier;

said seventh switch coupling said second memory element to said second input terminal of said differential gain amplifier;

said eighth switch coupling said fourth memory element to said second input terminal of said differential gain amplifier;

5. (Currently amended) In a semiconductor imaging chip having an array of active pixel sensors arranged in rows and columns, and an output bus terminal, a plurality of multiplexed column buffers, each of said plurality of multiplexed column buffers being coupled to a group of columns, each of said plurality of multiplexed column buffers comprising:

respective first, second, third and fourth ~~and second~~ memory elements;

respective first, second, third and fourth ~~and second~~ switches;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

a bus driver amplifier having respective input and output terminals;

said first memory element being selectively coupled to a first column of said array of active pixel sensors to store an active pixel sensor signal value for said first column;

said second memory element being selectively coupled to said first column of said array of active pixel sensors to store an active pixel sensor reset value for said first column;

said ~~second~~ third memory element being selectively coupled to a second column of said array of active pixel sensors to store an active pixel sensor signal value for said second column;

said fourth memory element being selectively coupled to said second column of said array of active pixel sensors to store an active pixel sensor reset value for said second column;

said first and third switches selectively coupling said first and third memory elements to said first input terminal of said differential gain amplifier during a first time intervalbus ~~driver amplifier~~;

said second and fourth switches selectively coupling said second and fourth memory elements to said input terminal of said differential gain amplifier during a second time interval; ~~bus driver amplifier; and~~

said output terminal of said differential gain amplifier being selectively coupled to said input terminal of said bus driver amplifier; and

said output terminal of said bus driver amplifier being selectively coupled to said output bus terminal of said semiconductor imaging chip to sequentially readout corrected active pixel sensor values for said first and second columns.

6. (Canceled)

7. (Currently amended) A multiplexed column buffer for use in a semiconductor imaging chip including an array of active pixel sensors arranged in rows and columns, said semiconductor imaging chip having an output terminal, said multiplexed column buffer comprising:

respective first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth ~~memory elements~~switches;

respective first, second, third, fourth, fifth and sixth ~~switches~~memory elements;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

a bus driver amplifier having respective input and output terminals;

said first switch coupling said first memory element to a first column of said array of active pixel sensors;

said second switch coupling said second memory element to ~~the~~ said first column of said array of active pixel sensors;

said third switch coupling said third memory element to ~~said~~ a second column of said array of active pixel sensors;

said fourth switch coupling said fourth memory element to said second column of said array of active pixel sensors;

said fifth switch coupling said first memory element to said first input terminal of said differential gain amplifier;

said sixth switch coupling said third memory element to said first input terminal of said differential gain amplifier;

said seventh switch coupling said second memory element to said second input terminal of said differential gain amplifier;

said eighth switch coupling said fourth memory element to said second input terminal of said differential gain amplifier;

said ninth switch coupling said fifth memory element to said output terminal of said differential gain amplifier;

said tenth switch coupling said sixth memory element to said output terminal of said differential gain amplifier;

said eleventh switch coupling said fifth memory element to said input terminal of said bus driver amplifier;

said twelfth switch coupling said sixth memory element to said input terminal of said bus driver amplifier; and

said output terminal of said bus driver amplifier being coupled to said output terminal of said semiconductor imaging chip.

8. (Canceled)

9. (Canceled)

10. (Currently amended) A semiconductor imaging chip comprising:

an array of active pixel sensors arranged in rows and columns;

an output terminal; ~~and~~

~~a multiplexed column buffer having a plurality of input terminals and a respective output terminal, said multiplexed column buffer further including a differential gain amplifier selectively connected to at least two of said plurality of input terminals so as to be multiplexed among at least two of said columns; wherein~~

~~said plurality of input terminals of said multiplexed column buffer is respectively coupled to said plurality of said columns and said multiplexed column buffer output terminal is coupled to said output terminal.~~

a first multiplexed column buffer having a first pattern cancellation circuit for providing a first corrected APS pixel signal value formed by the difference between an APS pixel signal value and an APS pixel reset value, said first multiplexed column buffer having at least two input terminals coupled to a first column and a second column respectively of said array of active pixel sensors, said first multiplexed column buffer having a respective output terminal to sequentially provide a corrected APS pixel signal value for said first column and a corrected APS pixel signal value for said second column;

a second multiplexed column buffer having a second pattern cancellation circuit for providing a second corrected APS pixel signal value formed by the difference between an APS pixel signal value and an APS pixel reset value, said second multiplexed column buffer having at least two input terminals coupled to a third column and a fourth column respectively of said array of active pixel sensors, said second multiplexed column buffer having a respective output terminal to sequentially provide a corrected APS pixel signal value for said third column and a corrected APS pixel signal value for said fourth column; and

said output terminal of said first multiplexed column buffers being sequentially coupled to said output terminal of said semiconductor imaging chip and said output terminal of said second multiplexed column buffers being sequentially coupled to said output terminal of said semiconductor imaging chip so as to sequentially readout corrected APS pixel signal values for said first, second, third and fourth columns of said array of active pixel sensors at said output terminal.

11. (Canceled)